Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended): A unity gain driver amplifier for driving an output node that is connected to a capacitive load, comprising:

a first stage amplifier for driving an intermediate node, a positive voltage input node for being connected to an input voltage and a negative input node for receiving a feedback signal;

a complimentary output stage having an input connected to said intermediate node and an output connected to the output node, a voltage representative of the voltage on the output node fed back to the negative input of said first stage amplifier; and

isolation circuitry for isolating the output node from said negative input node of said first stage amplifier as to prevent changes in phase shift due to large values of the capacitive loading during operation of the driver amplifier.

2. (Currently Amended): The driver amplifier of Claim 1, wherein the capacitive load comprises a capacitor array having a plurality of switched capacitors associated therewith that, during the operation of the driver amplifier, have one plate thereof connected to the output of the driver amplifier and the other plate thereof switched between two different ~~voltage~~ voltages in various combinations.

3. (Previously Presented): The driver amplifier of Claim 2, wherein the capacitors in the capacitor array are weighted capacitors.

4. (Previously Presented): The driver amplifier of Claim 3, wherein the weighted capacitors are binary weighted.

5. (Previously Presented): The driver amplifier of Claim 2, wherein the driver amplifier and the capacitor array are associated with an analog-to-digital converter that utilizes a SAR algorithm to perform a SAR search operation during a SAR conversion cycle so as to selectively switch the other plates of the capacitors between the two voltages in accordance with a search algorithm during the search operation.

6. (Previously Presented): The driver amplifier of Claim 1, wherein the positive voltage input node on said first stage amplifier comprises a high impedance input that is driven by a high impedance voltage generator to provide said input voltage thereto.

7. (Previously Presented): The driver amplifier of Claim 1, wherein said first stage amplifier comprises:

a current source for driving current from a first supply node to a common node;

a first current driver leg for driving current from the common node to a second supply node opposite in polarity to the first supply node, said first current leg responsive to said input voltage on said positive voltage input node such that current is increased through said first current driver leg as said input voltage moves toward said second supply node and decreases as said input voltage moves toward said first supply node; and

a second current driver leg for driving current to said intermediate node and sinking current from said intermediate node through a current path between said common node and said second supply node, the current there through controlled by the voltage on said negative input node such that an increase in the voltage on said negative input node will cause a decrease of current there through and a reduction in the voltage on said intermediate node and as the voltage on such negative input node moves toward said second supply node, the current through said second current path increases and the voltage on said intermediate node increases.

8. (Currently Amended): The driver amplifier of Claim 1, wherein said isolation circuitry comprises a feedback transistor having the source/drain path thereof connected between said intermediate node and said negative input node of said first stage amplifier in a diode-connected configuration with the gate thereof connected to said intermediate node and an output transistor ~~driving~~ having the source/drain path thereof connected between said output node and ground and the gate thereof connected to said feedback transistor, such that current can be sinked from said output node and the associated capacitive load with the voltage on said negative input node of said first stage amplifier substantially equal to the voltage on said output node.